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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|----------------------|------------------|
| 10/699,092 | 10/31/2003 | David Allen Brown | 8-1 | 2608 |
| 7590 | 12/28/2007 | | EXAMINER | |
| Ryan, Mason & Lewis, LLP 90 Forest Avenue Locust Valley, NY 11560 | | | EL CHANTI, HUSSEIN A | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2157 | |
| | | | MAIL DATE | DELIVERY MODE |
| | | | 12/28/2007 | PAPER |

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

| | | |
|------------------------------|------------------------|---------------------|
| Office Action Summary | Application No. | Applicant(s) |
| | 10/699,092 | BROWN ET AL. |
| | Examiner | Art Unit |
| | Hussein A. El-chanti | 2157 |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 31 October 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-20 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____. |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____. | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

1. This action is responsive to application filed on Oct. 31, 2003. Claims 1-20 are pending examination.

Drawings

2. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the drawings are informal. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Ng et al., U.S. Patent Application Publication No. 2004/0049564 (referred to hereafter as Ng).

As to claims 1, 19 and 20, Ng teaches an apparatus and a method for use in a processor for controlling access of a plurality of processor clients to a plurality of

memory instances of an internal memory of the processor, the apparatus and method comprising:

an internal memory controller comprising a configurable switching element (see paragraph [0036-0038] and fig. 2, the VSX are connected between the servers and the storage devices);

the configurable switching element being connectable between the plurality of clients and the plurality of memory instances and being operative to control access of particular ones of the plurality of clients to particular ones of the plurality of memory instances (see paragraph [0036-0038] and fig. 2, the vsx controls access to the storage devices);

wherein the configurable switching element is configurable to connect any one of at least a subset of the plurality of clients to each of at least a subset of the plurality of memory instances, such that in a first selectable configuration of the configurable switching element, a given one of the processor clients is permitted to access a first set of memory instances comprising one or more of the plurality of memory instances, and in a second selectable configuration of the configurable switching element, the given processor client is permitted to access a second set of memory instances comprising one or more of the plurality of memory instances, the second set being different than the first set (see paragraph [0036-0039], multiple servers are connected to multiple storage devices).

As to claim 2, Ng teaches the apparatus of claim 1 wherein the configurable switching element comprises a configurable crossbar having a first set of ports coupled to the plurality of processor clients and a second set of ports coupled to the plurality of memory instances (see paragraph [0040], the VSX comprises a plurality of ports that connects the servers to the storage devices).

As to claim 3, Ng teaches the apparatus of claim 1 wherein the memory controller further comprises control circuitry operative to control selection of a particular configuration for the configurable switching element (see paragraph [0036-0038] and fig. 2).

As to claim 4, Ng teaches the apparatus of claim 3 wherein the control circuitry further comprises an address control circuit (see paragraph [0030] and [0046]).

As to claim 5, Ng teaches the apparatus of claim 3 wherein the control circuitry further comprises a data multiplexing control circuit (see fig. 2).

As to claim 6, Ng teaches the apparatus of claim 1 wherein the internal memory controller further comprises a configuration interface providing an interface between the configurable switching element and a configuration source external to the memory controller, the external configuration source providing to the memory controller information utilizable to control selection of a particular configuration for the configurable switching element (see paragraph [0066-0067]).

As to claim 7, Ng teaches the apparatus of claim 1 wherein the plurality of processor clients comprises N processor clients, and the plurality of memory instances comprises M memory instances, where N need not be equal to M (see fig. 2).

As to claim 8, Ng teaches the apparatus of claim 7 wherein N is less than M (see fig. 2).

As to claim 9, Ng teaches the apparatus of claim 1 wherein the configurable switching element is configurable to connect any one of the plurality of processor clients to any set of memory instances comprising one or more of the plurality of memory instances (see paragraph [0066-0067]).

As to claim 10, Ng teaches the apparatus of claim 1 wherein for a given configuration of the configurable switching element, each of at least a subset of the memory instances has one and only one of the processor clients assigned to it (see paragraph [0036-0038] and fig. 2).

As to claim 11, Ng teaches the apparatus of claim 1 wherein addresses are allocated to multiple memory instances associated with the given processor client in order of decreasing memory instance size(see paragraph [0035]).

As to claim 12, Ng teaches the apparatus of claim 1 wherein multiple memory instances associated with the given processor client have different sizes which are related to one another as multiples of two(see paragraph [0035]).

As to claim 13, Ng teaches the apparatus of claim 1 wherein a different set of mask bits is associated with each of a plurality of different memory instance sizes, and a different address decoder value is associated with each of the plurality of memory instances (see paragraph [0056-0057]).

As to claim 14, Ng teaches the apparatus of claim 13 wherein address decoding logic applies the mask bits for a given memory instance to an incoming address from the given processor client, and compares the result to the address decoder value for the given memory instance to determine if the incoming address is directed to an address in the given memory instance (see paragraph [0056-0057]).

As to claim 15, Ng teaches the apparatus of claim 14 wherein a decoded address is considered valid for the given processor client only if a master client identifier stored for the given memory instance specifies the given processor client (see paragraph [0056-0057]).

As to claim 16, Ng teaches the apparatus of claim 1 wherein the processor is configured to provide an interface for communication of protocol data units between a network and a switch fabric (see paragraph [0057-0058]).

As to claim 17, Ng teaches the apparatus of claim 1 wherein the processor comprises a network processor (see fig. 2).

As to claim 18, Ng teaches the apparatus of claim 1 wherein the processor is configured as an integrated circuit (see fig. 2).

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

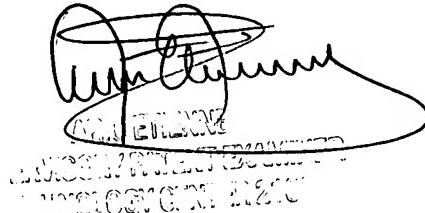
5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hussein A. El-chanti whose telephone number is (571)272-3999. The examiner can normally be reached on Mon-Fri 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Etienne can be reached on (571)272-4001. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hussein Elchanti

Dec. 21, 2007



The image shows a handwritten signature "Hussein Elchanti" written over a printed nameplate. The nameplate contains the text "USPTO", "Patent and Trademark Office", "U.S. DEPARTMENT OF COMMERCE", and "2000 C. K St., N.W., Washington, D.C. 20591".